AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to FIGS. 1, 4, 5, and 6, in which descriptive labels have been added. No new matter is added.

Attachment: Replacement sheets

REMARKS

Claims 1-17 are pending in the application.

The drawings were objected to. FIGS. 1, 4, 5, and 6 have been amended to include descriptive labels. No new matter has been added. Approval of the replacement drawing sheets and withdrawal of the objections are respectfully requested.

The specification was objected to. The abstract has been amended to include between 50 and 150 words. The word "means" has been removed. The specification has been amended to conform to preferred layout, including the addition of appropriate section headings. No new matter has been added. Withdrawal of the objection is respectfully requested.

Claims 1-14 and 16 were rejected under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 5,708,684 to Ueda ("Ueda"). Claims 15 and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ueda in view of U.S. Patent No. 4,392,220 to Hirosaki et al. ("Hirosaki"). These rejections are respectfully traversed.

Applicants' claimed invention is directed to a method, a phase detector, and a device for controlling the phase of successively transmitted frames in which data symbols are transmitted at a constant symbol frequency (see, e.g., independent claims 1, 11, and 12). As claimed, the data symbols are grouped together in frames, and "the phase of the frame transmission is controlled so that the frames are transmitted on average synchronously with the data clock" (independent claim 1; see also claims 11 and 12).

For example, as recited in independent claim 1, a phase difference between the clock of the frame transmission and a data clock is determined. The data clock measures the frequency at which the data symbols to be transmitted arise, or the data source frequency (see, e.g., specification at page 1, lines 32-34).

As claimed, depending on the phase difference, an adjusting signal is produced for controlling the injection of stuffing data symbols into the frames for changing the frame length and the phase of the frame transmission, and through this injection of stuffing data symbols, the phase of the frame transmission is controlled so that the frames are transmitted on average synchronously with the data clock (see independent claims 1, 11, and 12).

Further, as recited in independent claims 1, 11, and 12, the adjusting signal is produced dependent on a phase difference determined from N successively transmitted frames, wherein N is at least equal to two. In other words, the adjusting signal depends not only on the phase difference between the clock of the frame transmission and the data clock, but also on a second phase difference for N successive frames.

In the Action, the Background section of Ueda was cited (see, e.g., columns 1 and 2 of Ueda). However, the Background section of Ueda describes the prior art, and is not related to the cited passages in columns 7-12 of Ueda.

For example, in columns 1 and 2, Ueda describes the transmission of signals for a transmitter in radio equipment. The data is transmitted as frames (also referred to as multi-frames) which are composed of 30 sub-frames or timeslots, and each sub-frame is composed of one bit of control data (overhead bit) and seven bits of information data. A stuffing bit may be inserted into the 30th sub-frame (see column 1, lines 43-48 of Ueda). As explained in column 1, line 54 - column 2, line 6, a stuffing bit is inserted to match the data input rate and the data output rate, and when no stuffing bit is inserted data is inserted. The greater the difference between the data input rate and the data output rate, the greater the number of stuffing bits inserted is, while the smaller the difference the smaller the number. This passage relates to the structure of FIG. 34 of Ueda (see column 1, line 23) where no phase detector or the like is shown. Furthermore, in the Background section of Ueda, no information is provided on how the difference between the data input rate and the data output rate, and thus the number of stuffing bits to be inserted in the 30th sub-frame, is determined.

The remaining cited passages of Ueda do not teach or suggest the injection or insertion of stuffing bits or stuffing data symbols as recited in independent claims 1, 11, and 12. In particular, Ueda describes, in column 4, lines 30-55, the enabling of a seamless switching between an active radio transmitter and a standby radio transmitter, for which the phases of the transmitters have to be matched. Consequently, Ueda describes radio equipment comprising two radio transmitters the delays and phases of which are made coincident (see Ueda, column 7, lines 40-52). Therefore, as explained in column 8, lines 34-48 of Ueda, a phase comparator is provided in a receive data processing unit so as to compare the phases of a frame data signal and a clock signal which are received from the standby radio receiver with the phases of a frame data signal and a clock signal which are directly received from the transmitting data processing unit. A delay time adjuster is widened on the basis of the phase comparison.

Ueda does not teach or suggest <u>determining a phase difference between a clock of the frame transmission and a data clock</u>. Instead, in Ueda, a phase difference is determined between a frame data signal from a standby radio receiver and a frame data signal from a transmitting data processing unit, and a phase difference between a clock signal from a standby radio receiver and a clock signal from a transmitting data processing unit (see, e.g., FIG. 1 and column 12, lines 1-11 of Ueda). Thus, Ueda does not teach or suggest comparing a frame data signal with a clock signal to determine a phase difference.

In Ueda, the insertion of stuffing data symbols is <u>not</u> controlled by an adjusting signal produced depending on the phase differences. Instead, in Ueda, the phase differences are used to control delay time adjusters (see, e.g., column 8, lines 42-48 and column 12, lines 34-38 of Ueda), which is clearly different from the injection of stuffing data symbols into the frames for changing the frame length and the phase of the frame transmission as recited in independent claims 1, 11, and 12.

Further, Ueda does not teach or suggest that the adjusting signal is produced depending on the phase difference determined from N successively transmitted frames.

Rather, Ueda describes that the delay time adjusters are adjusted depending on the phase differences, as described above.

For at least the reasons discussed above, Ueda does not anticipate or otherwise render obvious the Applicants' claimed invention. Therefore, independent claims 1, 11, and 12 and their respective dependent claims are patentable over Ueda.

Furthermore, neither Ueda nor Hirosaki, alone or in combination, disclose all the elements of claim 15 and 17. Each of claims 15 and 17 depend from claim 12. As described above, Ueda does not teach or suggest the limitations of claim 12. Hirosaki does not cure this defect of Ueda. Instead, Hirosaki describes the use of a differential amplifier in integrated circuits for a modem used with spread spectrum, multiplex communications networks (see Hirosaki, column 54, starting at line 60). Even if Hirosaki was somehow combined with Ueda, the proposed combination would not produce the Applicants' claimed invention, for at least the reasons discussed above.

In view of the above amendment, applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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Attachments